

MICROELECTRONIC DEVICE RELIABILITY

FINAL REPORT

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INTRODUCTION

Very Large Scale Integrated (VLSI) circuits play an important role in modern military technology. When used in military equipments operated over a very wide variety of environmental conditions, their long term ability to function as designed, i.e. their reliability, is an important attribute. In recent years the rapid evolution of solid-state device technology that has culminated, to date, in VLSI has driven the semiconductor industry to ever shorter product life cycles. There is no longer any time for the "learning curve" from the analysis of failed devices (field returns) to feed back into design and manufacturing to improve reliability. Now reliability must be both designed-in and built-in. To do so requires understanding of the physical mechanisms leading to failure and a translation of that understanding into guidelines for designers and fabricators.

The Army Research Office recognized this need when it granted support to Clemson University to establish an ARO Fellowship to be awarded to a qualified U.S. citizen pursuing a PhD program specializing in research on the reliability of microelectronic devices.

RESEARCH ACTIVITIES

A VLSI reliability research program has been on-going in the Center for Semiconductor Device Reliability Research at Clemson University since 1983. This has been supported primarily by the Semiconductor Research Corporation with additional support from several of the member companies of that organization. This program includes research in: charge injection into thin oxides; electrostatic discharge; electromigration; and the development of computer-aided-design (CAD) tools for assessment of reliability at the design stage.

Mr. Alan S. Lewis started work on a PhD program in the Electrical and Computer Engineering Department at Clemson University in the Fall semester of 1986. He was selected from several qualified applicants. Support on the ARO Fellowship initiated by this Grant (DAAL03-86-G-0066) commenced 15 August 1986. Mr. Lewis elected to do research on the failure mechanism of electromigration and began research work under the direction of Professor James W. Harrison, Jr. at this time.

Mr. Lewis was assigned the research goal of developing a simulation model for electromigration damage in a metallization line on a VLSI chip, an increasingly important reliability problem. He was to use as the basis of his work a first order model already developed by Professor Harrison and extend it to take into account various additional stressors other than electric current, e.g. mechanical stresses and gradients due to the differing thermo-mechanical properties of the metallization, the dielectric under- and over-layers and the silicon substrate. The objectives of this development were:

1. To gain insight into the effects of various physical factors on electromigration damage rates and to use this insight to guide the development of more reliable IC devices; and
2. To provide modeling tools that can be utilized ultimately in computer-

aided-design (CAD) of reliable IC devices.

Mr. Lewis was first assigned to do an extensive review of pertinent technical and scientific literature on electromigration and its technical consequences. Following this, he was assigned the task of critically reviewing the existing simulation model. Then he was assigned the task of working with two other graduate students under Professor Harrison's direction to become acquainted with the design features and operation of a computer-controlled data acquisition system which was being used to collect test data on pulsed current electromigration effects in test lines donated by an industrial source (Harris Semiconductor).

During the latter assignment Mr. Lewis conceived the idea of designing a test chip containing electromigration test lines that would better match the pulse driving system being used. In this system a stripline configuration was being used on the polyimide based printed circuit board being used for accelerated testing at high temperature (up to 230 degrees C). The stripline had a characteristic impedance of about 100 ohms and "padding resistors" had to be used with the sample lines being tested. Subsequently, during the summer of 1987, Mr. Lewis was employed by the General Electric (now Harris Semiconductor) Microelectronics Center in the Research Triangle Park (hereinafter called the GEMC-RTP) where he was encouraged to use their CAD facilities to implement the design. This was done by August of 1987, when he returned to Clemson University to continue his school work. These test lines were a significant improvement over those previously used in that they had Kelvin contacts for potential probing, a tapered design to mitigate high temperature gradient end effects [1], and had a nominal resistance of about 100 ohms at 200 degrees C, which provided a good impedance match to the pulse drive circuitry and stripline on the test boards.

During the Fall of 1987 Mr. Lewis continued to familiarize himself with the details of electromigration testing, which would be used to develop data for model validation, and with maintaining a close liaison with GEMC-RTP to initiate and monitor a limited fabrication run of the new test line design. GEMC-RTP had generously agreed to help support the reliability research program at Clemson University by making these devices. The test chips, mounted in ceramic 24 pin DIP packages were received in late December, 1987.

Early in 1988 Mr. Lewis began the task of electrical and thermal characterization of these samples in preparation for DC baseline electromigration testing prior to high frequency (2MHz to 10 MHz) pulse testing. This work was well along when Mr. Lewis, for personal reasons, decided to cut short his work on a PhD and to go to work as a full-time employee of the GEMC-RTP. His departure from the Clemson University reliability research program was a real loss to this program, although he continued to be a staunch supporter of our program and was instrumental in obtaining for us a second, even larger batch of advanced metallization material test structures employing his design.

ADMINISTRATIVE ACTIVITIES

Subsequent to Mr. Lewis's resignation from the ARO Fellowship in late March, 1988 the vacant position was publicized. An excellent prospect was identified and appeared willing to commit to a PhD program, a requirement for the award, but decided in August, 1988 to decline and work toward the limited objective of a Master of Science degree. Following this an effort was once again made to find a suitable candidate. On two subsequent occasions the prospects, both with excellent qualifications, also decided to decline the appointment, both hesitant to commit to a PhD program. After the last candidate declined, in March, 1989, it appeared that there was no subsequent interest by anyone who was:

1. Interested in a PhD program in VLSI reliability; and
2. A U.S. citizen.

This situation continued until the termination date of the grant.

REFERENCES

- [1] H. Schafft et al, "Reproducibility of Electromigration Measurements", IEEE Trans. Electron Devices, ED-34, 673 (1987).